World Applied Sciences Journal 32 (1): 104-110, 2014
ISSN 1818-4952

DOI: 10.5829/idosi.wasj.2014.32.01.841

# Direct Carry Array Multiplier: a New Approach to Lowpower and High Efficient Structure

*[1]Mohsen Sadeghi, [2]Jamal Rajabi and [3]Abbas Golmakani*

[1]Sadjad Institute for Higher Education, Mashhad, Iran
[2]Shahrood University of Technology, Shahrood, Iran
[3]Department of Electrical Engineering, Sadjad Institute for Higher Education, Mashhad, Iran

**Abstract:** In this article, we proposed a newly designed multiplier with low power consumption and high speed in processes based on a new structure. Due to increasing demand for integrated circuits with being higher in speed, lower in delays, higher in power efficiency as well as more compact in size, we decided to design a new structure to enhance the mentioned characteristics. It is common to use adder units in designing digital multiplier cells and here it has been used the same method.In our proposed structure has been utilized of 4×4-bit adder units since it is the base structure in digital multipliers. The main merits of this multiplier are the least adder unit count, ultra-low power consumption and propagation delay in comparison with other structures. Here, some of the most prevalent multiplier structures such as Array multiplier, RCA multiplier, Braun multiplier, Bypassing RCA, Bypassing CSA have been simulated in HSPICE software by using 28T full adder cell; At the next stage, a comparison among them and hence our proposed multiplier has been applied. As it can be figured out from the comparison results, the proposed structure enjoys the best performance in terms of power consumption, propagation delay, throughput and latency compared to the other simulated structures. The figures demonstrates that the proposed structure consumes 25% less power than Bypassing RCA multiplier (the lowest power consumer among the rest of mentioned structures), moreover, its propagation delay and adder units count are respectively 36.15% and 16.7% lower than Bypassing RCA multiplier. Note that all of these simulations have been carried out by HSPICE in 0.18 m technology at 1.8V supply voltage. To make along story short, our proposed design is the best choice to fit in low power and high speed arithmetic applications.

**Key words:** Propagation Delay · RCA Multiplier · Braun Multiplier · Bypassing RCA and Bypassing CSA

## INTRODUCTION

As we march on through this technology-driven century with the evolution of the shrinking technology, demanding laptops and other personal portable communication systems with higher speed in processing and more battery lifetime are growing drastically. Hence, the researchers have intensified their endeavors to attain this goal.

Nowadays, the lower in power consumption circuits are the more qualified candidates they will be in microprocessors and system-components applications [1-4]. On one hand, the increasing growth of the electronics market has driven the VLSI industry towards very high integration density and system on chip designs alongside beyond few GHz operating frequencies and on the other hand, critical measures should be taken into account due to severe increase in power consumption and the need of reducing it further [5].

There exist some major operations involved in digital computer systems and digital signal processing which multiplication is the most important operation among them. Reducing power dissipation of multipliers are considered as power hungry components and literally leads to the reduction of overall power budget of digital VLSI circuits. To achieve such a difficult goal, some method can be applied internally or externally. As far as internal techniques are concerned, they are associated

**Corresponding Author:** Mohsen Sadeghi, Sadjad Institute for Higher Education, Mashhad, Iran.

with architecture, logic and circuit designs of the multiplier, whilst external techniques deal with input data characteristics. As can be captured from above mentioned explanations, extending the operating hours of portable electronic device without choosing another battery with higher amount in capacity, is still the major concern. Although advanced technology has enhanced battery lifetimes, the complicated operations in the high-end portable devices are still power hungry and is critical for the low power design [6].

There are two different ways to design a multiplier: 1. Designing its overall structure and 2. Designing adder units of multiplier. Multipliers perform the all of the operations which are needed to be done by a portable electronic device. So they must be utilized maximally in terms of power, Propagation delay, throughput, EPI and latency [7], [8]. In recent years, a lot of tiny multiplier circuits have been designed offering lower power dissipation, propagation delay and power rating of input bits [7-9]. As for a complementary pass transistor logic circuit, the main source of power dissipation is the switching activity of its nodes, which may dedicate more than 90% of total power consumption to itself [8], [10] and [11]. There are five important factors which VLSI designer are always in challenge with: Power, delay, area, power delay product (PDP) and energy delay product (EDP). Among the mentioned factors, EDP is the most important parameter to be addressed for optimizing a VLSI circuit [12-14].

The total power dissipation in generic digital CMOS gate is calculated by following equations:

$$P_{Total}=P_{Dynamic}+P_{ShortCircuit}+P_{Static} \quad (1)$$

$$P_{Dynamic}=P.C_L.f.V_{DD}^2 \quad (2)$$

$$P_{ShortCircuit}=I_{peak}.t_{SC}.V_{DD}.f \quad (3)$$

$$P_{Static}=I_{Static}.V_{DD} \quad (4)$$

In the above equations $V_{DD}$, $C_L$, f, P, $I_{Static}$, $I_{peak}$ and $t_{SC}$ are respectively supply voltage, capacitor of gate, simulation frequency, change state probability of gate, static current, maximum current during changing the status of gate and short circuit time. Note that static power is very important in low supply voltages rather than high supply voltages.

There is a considerable delay between receiving inputs and delivering outputs, since several adder units exist along this path. Moreover, another harmful effect impacts on our data which is called glitch effect and causes a significant increase in power consumption. To overcome these problems, the researchers are compelled to reduce these adder units as much as possible. Our proposed design shows the implementation of a 4×4 bit multiplier circuit with minimum adder units' count among the other multipliers which have been introduced up to now.

The remaining of the paper is organized as follows: Section (2) is about a brief description of the 28T full adder cell. Objectives and scopes have been noted in section (3). Prior multiplier architectures are illustrated in Section (4). Explanations about the proposed multiplier are given in section (5) entitled materials and methods. The simulation results of the proposed multiplier structure and its performance comparisons with counterparts' multipliers are shown in Section (6). Section (7) discusses about the comparison results. Lastly, conclusion is given in Section (8).

**Conventional CMOS 28 Transistor (28T) Full Adder:** The 28 transistor full adder is the pioneer of CMOS traditional adder circuits. Figure 1 illustrates the schematic of the adder. The number of NMOS and PMOS transistors which has been used to produce this cell, are equal: 14 PMOS and 14 CMOS transistor. The main advantage of this adder is its excellent output swing.

**Objectives and Scopes:** Since the multiplication is the vital function in DSP processors and moreover, there exist great deals of applications today requiring these processors as the core of their systems, optimizing them will surely affects the overall performance of systems. The main objectives in this area are as follow:

- Increasing processing speed by reducing delay
- Decreasing propagation delay time as the most important factor amongst other types of delay by using the least adder units.
- Mitigating power consumption by attenuating glitch effect
- Achieving more integrity by using as least adder units as possible

The aim of this study was to introducing a new multiplier structure to meet the above-mentioned goals.

**Prior Works**

**Multiplier Architectures:** In fact, multipliers are complex arrays of adder units. This is a common operation to a large number of applications and the complexity of this

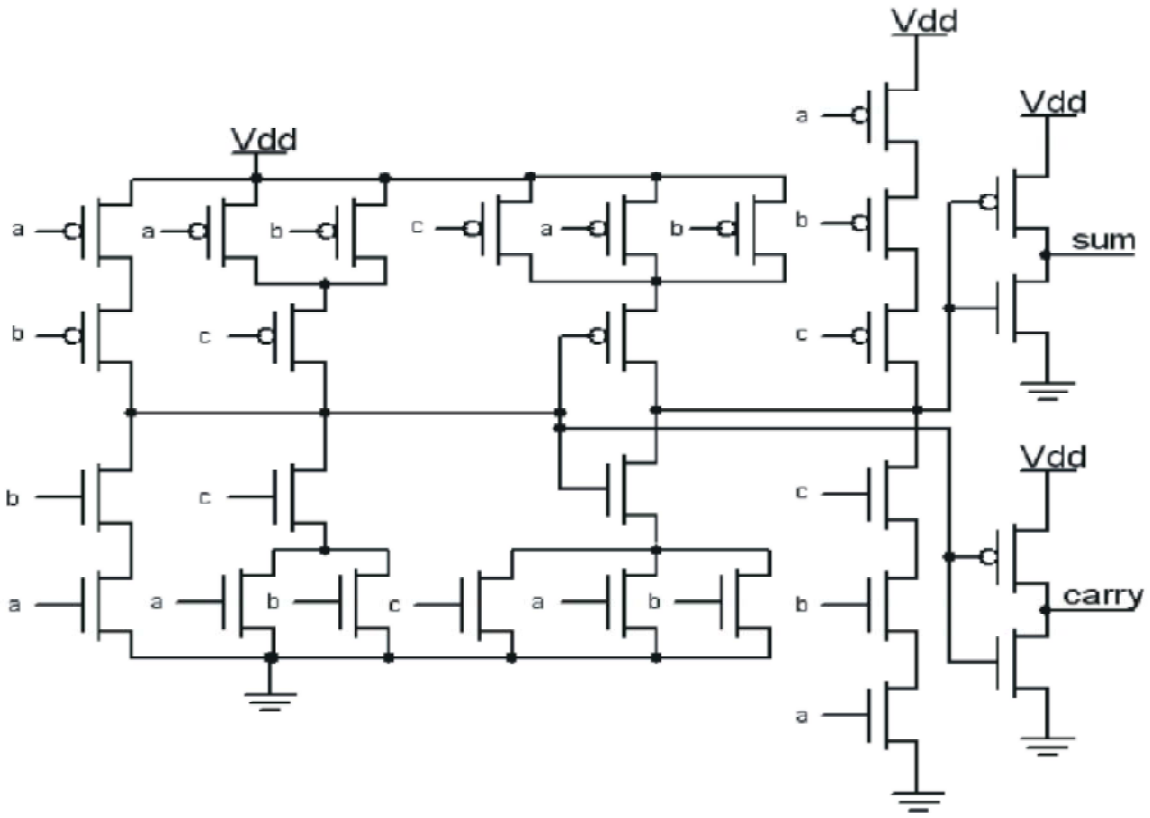


Fig. 1: Conventional CMOS Adder with 28 transistors

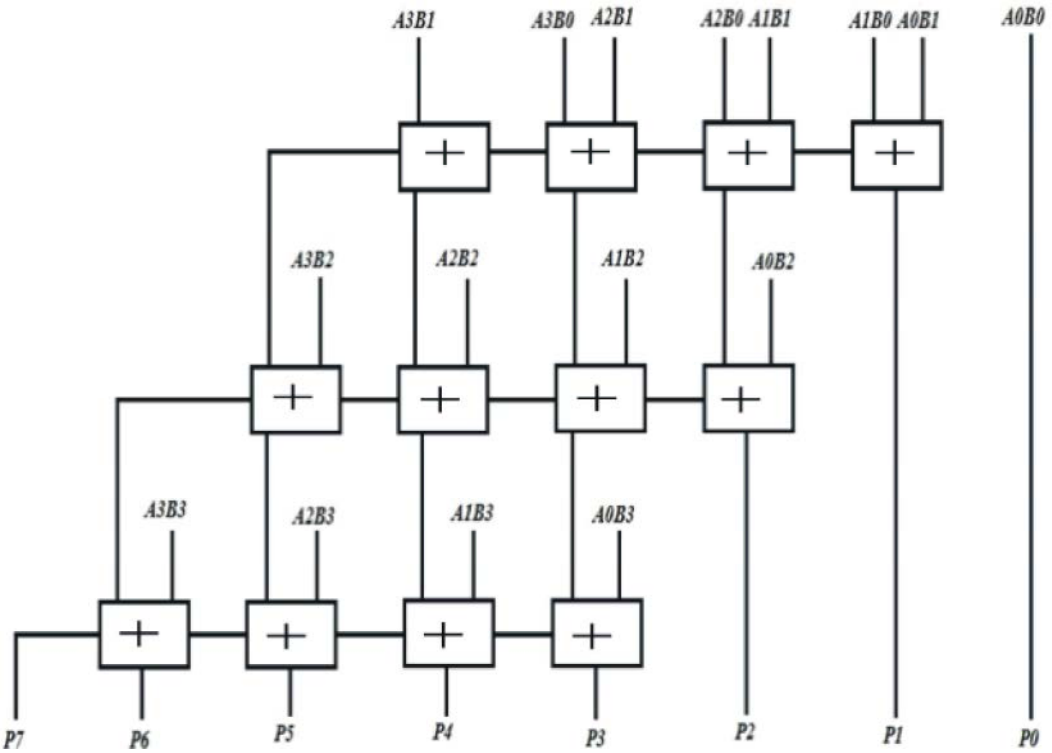


Fig. 2: 4×4 Bit Array Multiplier

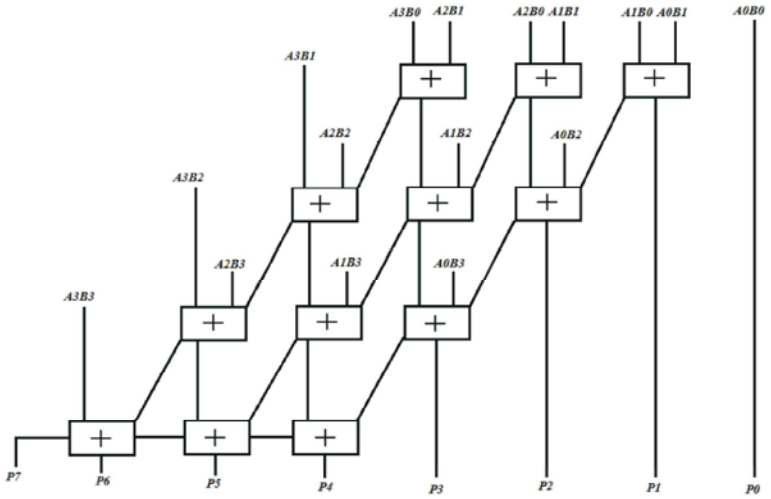


Fig. 3: 4×4 Bit Basic Braun Multiplier

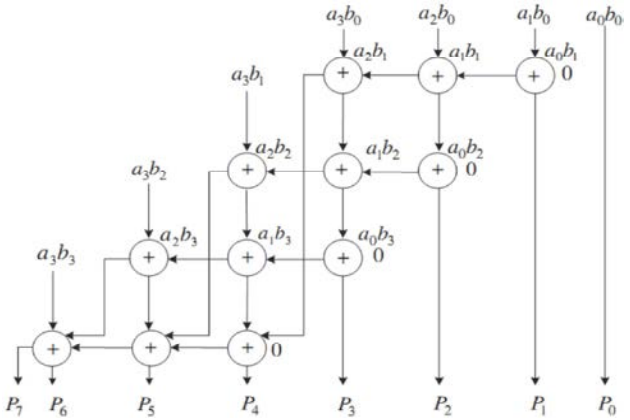


Fig. 4: 4×4 Bit Ripple Carry Array Multiplier (RCA)

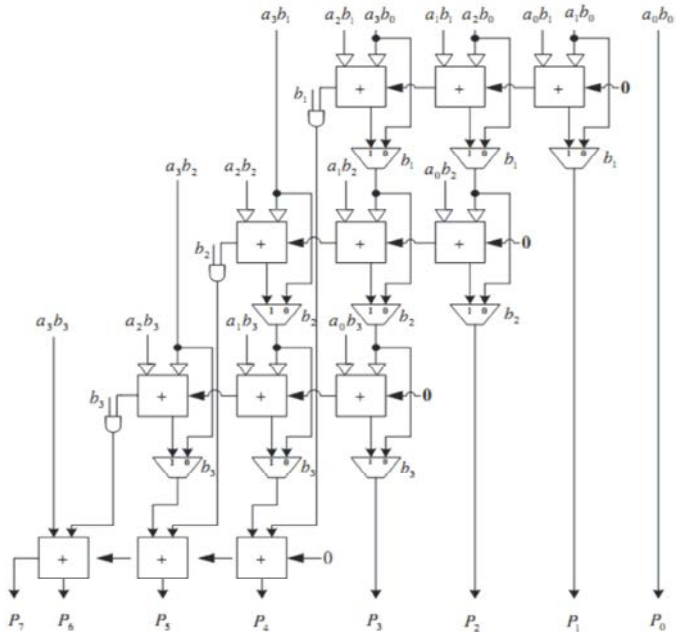


Fig. 5: 4×4 Bit Row Bypassing Multiplier based on RCA

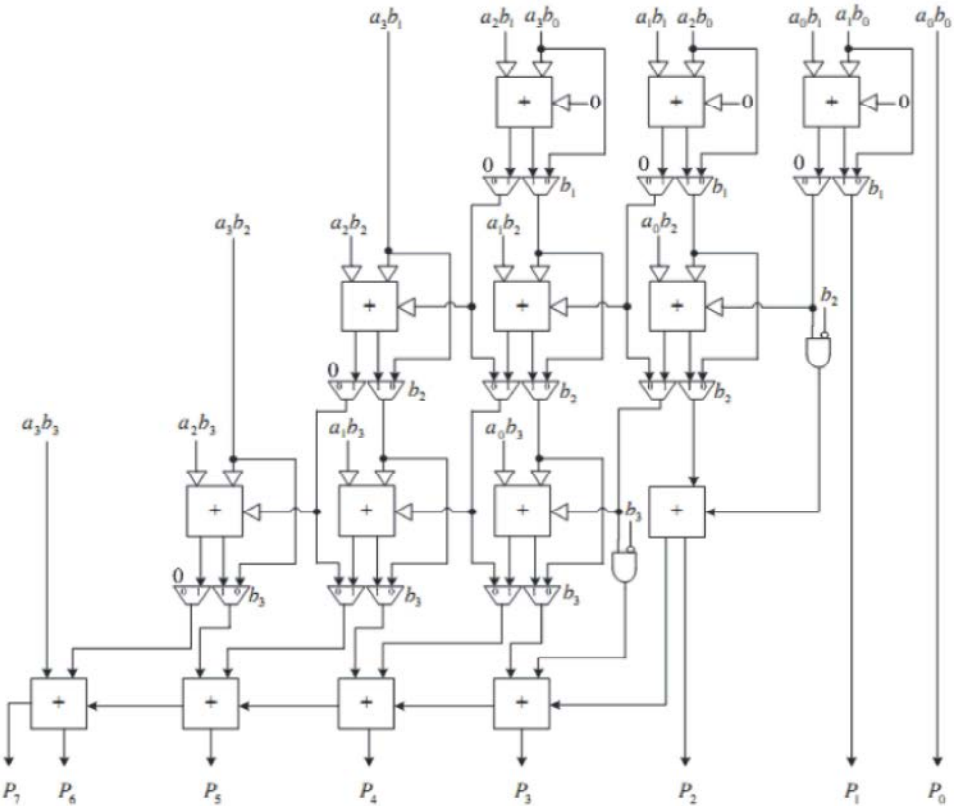


Fig. 6: 4×4 Bit Bypassing Multiplier based on CSA

function has led to a large amount of researches aimed at speeding up its execution. Multiplier can be implemented using different algorithms. Some of common structures of multipliers are as shown in Figure 2, Figure 3, Figure 4, Figure 5 and Figure 6.

## MATERIALS AND METHODS

**Proposed Multiplier Based on a New Structure (DCA Multiplier):** In this section, our new structure of multiplier (DCA) is presented. In this structure minimum adder units have been used; that's why it has the fewest transistor count than those of other structures. The Direct Carry Array Multiplier (DCA) has been designed as it has very low propagation delay and power consumption, so we achieve very low PDP and EDP.

The following steps were taken to design the DCA multiplier. First of all, it was necessary to find a logical relation between input and output bits. Then, it was important to attain a structure possessing the least high swing and ultra-low delay adder unitsalong the path from input to output which meets the requirements.

To choose the best full adder block in term of delay and swing properties, we compared some kinds of priorstructures and visited that 28 transistor full adder fits in our work better than others do. After doing these steps, it was simulated by HSPICE softwareto investigate the results and diagnosing the probable malfunctions.

As final step, the proposed circuit is evaluated and compared to the other ones. Comparisons have been done for major characteristics namely Average power, Delay, PDP, EDP and transistor count. All multipliers were simulated using 28T full adder cell in 0.18µm CMOS technology files with 100MHz and at 27°C and the supply voltage was 1.8 V.

Our proposed design has been illustrated in Figure 7.

## RESULTS

In this section, the simulation results of different multipliers and proposed multiplier (DCA multiplier) are tabulated below and the comparison chart has been given below that.

It is anticipated from the results that the DCA multiplier consumes the least power compare to the others. Moreover DCA multiplier has the lowest propagation delay, power delay product, energy delay product and occupied area than the other structures have.

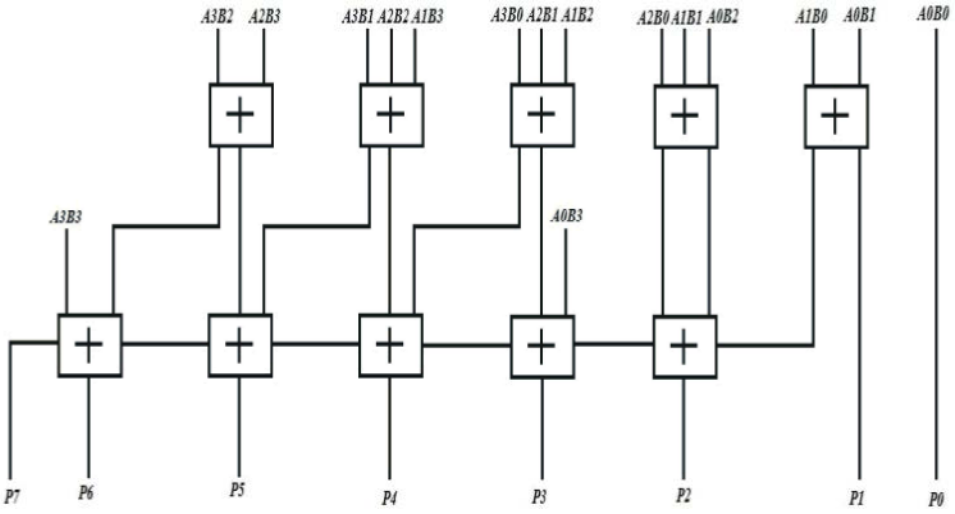


Fig. 7: 4×4 Bit Direct Carry Array Multiplier (DCA)

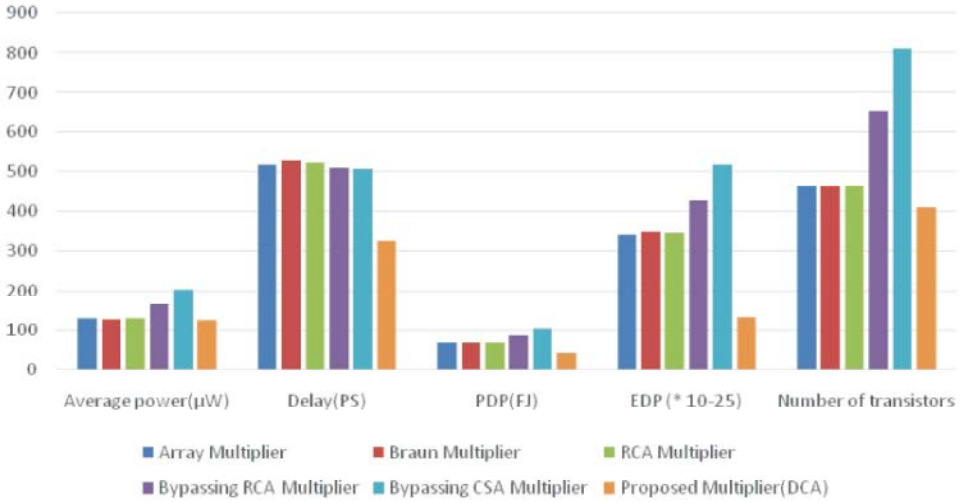


Fig. 8: Comparison results of afore-mentioned multipliers' characterization

Table 1: Simulation Results for 1.8v, 100MHz

| Design | Average power (µW) | Delay (PS) | PDP (FJ) | EDP (* $10^{-25}$) | Number of transistors |
|---|---|---|---|---|---|
| Array Multiplier | 126.66 | 517.5 | 65.54655 | 339.2033 | 464 |
| Braun Multiplier | 125.76 | 526.5 | 66.21264 | 348.6095 | 464 |
| RCA Multiplier | 126.60 | 521.5 | 66.0219 | 344.304 | 464 |
| Bypassing RCA Multiplier | 164.84 | 509 | 83.90356 | 427.069 | 655 |
| Bypassing CSA Multiplier | 202.3 | 505.5 | 102.2626 | 516.937 | 810 |
| Proposed Multiplier(DCA) | 123.69 | 325 | 40.19925 | 130.6475 | 408 |

## DISCUSSION

As far as the results are concerned, our proposed structure has possessed the most efficiency amongst the other ones. Here, we compared the results of DCA multiplier with Array multiplier which is of the best performance in comparison with another mentioned multipliers.

The DCA multiplier consumes approximately 2.5% less power than the Array multiplier does. In term of delay, our introduced structure responses above 37% faster compared to the other one. As regards to PDP, it is 38.7% less than the Array multiplier. Likewise, it has shown 61.5% better performance compared to the Array multiplier's in EDP parameter. Last but not least, it consisted of 408 transistors while the latter one has 464

transistors in itself which it means the occupied area by DCA multiplier is significantly lesser than the Array multiplier does.

Lastly, based on above results, the DCA multiplier is a new structure which has been succeeded to improve other multipliers' characterization toward achieving an efficient multiplier.

## CONCLUSIONS

In this paper a high performance and low power CMOS array multiplier was presented. There exist some major limitations in designing efficient multipliers such as gaining desired delay and swing. High delay leads to intensification glitch effect that increases static power consumption which takes us away from high efficient multiplier. Additionally, low output swing causes two main problems. Firstly, it may conclude to wrong outputs and the other problem appears when it exceeds regular power consumption. The proposed multiplier decreases power consumption and propagation delay by removing extra adder units. This work primarily focused on the designing multiplier using minimum adder units with the least possible propagation delay. Intensively, HSPICE simulation proved that the new structure possessed the lowest power consumption, propagation delay, PDP, EDP. These results were obtained with simulating by HSPICE software at room temperature and 1.8V as a supply voltage. In the future works, we aimed at designing a multiplier with carry bit prediction in order to lower delay factor. In this case, we manage to attain a multiplier owning superb features[15].

## REFERENCES


1. Shalem, R., E. John and L.K. John, 1999. "A novel low-power energy recovery full adder cell," in Proc. Great Lakes Symp. VLSI, pp: 380-383.
2. Chandrakasan, A.P., S. Sheng and R.W. Broderson, "Low-power CMOS digital design," IEEE J. Solid-State Circuits, 27: 473-483.
3. Pedram, R. and M. Pedram, 1996. Low Power Design Methodologies. Norwell, MA: Kluwer.
4. Jiang, Y., A. Al-Sheraidah, Y. Wang, E. Sha and Jin-Gyun Chung, 2004. "A Novel Multiplexer-Based Low-Power Full Adder," IEEE Transaction on Circuits and Systems, pp: 51.
5. Abid, Z., H. El-Razouk and D.A. El-Dib, 2008. "Low-power multipliers based on new hybrid full adders," Microelectronics Journal, pp: 1509-1515.
6. Ko-Chi, Kuo and Chi-Wen Chou, 2010. "Low power and high speed multiplier design with row bypassing and parallel architecture," Microelectronics Journal, 41: 639-650.
7. Ying, J., F. Tong, D. Nagle and R.A. Rutenbar, 2000. "Reducing power by optimization the necessary precision, range of floating-point arithmetic," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., 8(3): 273-286.
8. Senthilpari, C., A.K. Singh and K. Diwakar, 2008. "Design of a low-power, high performance, 8*8 bit multiplier using a Shannon-based adder cell," Microelectronic Journal, 39: 812-821.
9. Hsiao, S.F., J.S. Yeh and D.Y. Chen, 2002. "High-performance multiplier based logic synthesis using pass-transistor logic," VLSI Design, 15(1): 417-426.
10. Nguyen, H.T. and A. Chatterjee, 2000. "Number-splitting with shift-and-add decomposition for power and hardware optimization in linear DSP synthesis," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., 8(4): 419-424.
11. Soudris, D., C. Piguet and C.G. Esigning, 0000. "CMOS Circuits For Low power," European Low-Power Initiative for Electronic System Design, Kluwer Academic Publishers, Boston/Dordrecht/London.
12. Sadeghi, M., M. Ali and A. Golmakani, 2014. "Binovel Low-Power and High Performance Full-Adder Cell In 180nm Cmos Technology," World Applied Sciences Journal, 31: 240-243.
13. Sadeghi, M., J. Rajabi and A. Golmakani, 2013. "Novel 1-Bit Full-Adder Cell with Ultra-Low Delay, PDP and EDP," International Journal of Management, Information Technology and Engineering (BEST: IJMITE), 1: 1-4.
14. Sadeghi, M., J. Rajabi and A. Golmakani, 2014. "A novel low-power 1-Bit CMOS full-adder cell based on multiplexer," International Journal of Computer Science Engineering (IJCSE), 3: 77-80.