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Ultra-High Speed Multiplier Based on a Novel Structure

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***Abstract*— This paper presents a low power and high speed multiplier based on a novel structure. Which the main advantage this structure has the lowest adder unit count, consumption power, and propagation delay. In this paper is simulated some of common structures of multiplier by using 28T full adder cell. We have compared some of the most common multiplier structures like Array multiplier, RCA multiplier, Braun multiplier, Bypassing RCA, Bypassing CSA, and proposed structure of multiplier. From the analysis of these simulated results, it was found that the proposed multiplier structure gives the best performance in terms of power, propagation delay, latency and throughput than other published results. Intensively, HSPICE simulation shows that the new structure consumes 24% less power than Bypassing RCA multiplier, moreover its propagation delay and adder units count 31.63% and 8.34% lower than Bypassing RCA multiplier respectively. Simulation has been carried out by HSPICE in 0.18µm technology at 1.8V supply voltage. The proposed design is suitable for low power and high speed arithmetic applications.**

Keywords-Propagation Delay; RCA Multiplier; Braun Multiplier; Bypassing RCA; Bypassing CSA

I. INTRODUCTION

With the explosive growth in laptops, portable personal communication systems, and the evolution of the shrinking technology, the research effort in low-power microelectronics has been intensified. Today, there are an increasing number of portable applications requiring small-area low-power high throughput. Therefore, circuits with low-power consumption become the major candidates for design of microprocessor and system-components [1-4]. While the growth of the electronics market has driven the VLSI industry towards very high integration density and system on chip designs and beyond few GHz operating frequencies, critical concerns have been arising to the severe increase in power consumption and the need to further reduce it[5].

Multiplication is one of the most important operations in digital computer systems and digital signal processors. Besides, multipliers are power hungry components, so reducing their power dissipation is a key to satisfying the overall power budget of digital VLSI circuits. Various techniques can be applied externally or internally techniques deal with input data characteristics, whereas internal techniques are concerned with the architecture, logic and circuit designs of the multiplier [5]. The primary concern of electronic portable device is to extend operating hours without changing the battery residing in device. Although advanced technology enhanced battery life to operate for longer hours, the complicated operations in the high-end portable devices are still power hungry and is critical for the low power design [11].

For designing multipliers two ways exist, the first way is design of overall structure it and the other way is design of adder units of multiplier. In electronic devices applications, multipliers perform all of the operations and are needed for maximum utilization of power, propagation delay, throughput, EPI and latency [6], [7]. In recent years, many small-sized multiplier circuits have been proposed that offer lower propagation delay, low-power dissipation and low-power rating of input bits [6-8]. Since power consumption determines the time between two successive recharges of such a device, as well as the device's battery life, the reduction of power dissipation is vital in such devices. The main source of power dissipation in a complementary pass transistor logic circuit is the switching activity of its nodes, which may contribute to more than 90% of the total power consumption [7], [9], and [10]. The five important considerations for VLSI design are power, delay, area, power delay product (PDP) and energy delay product (EDP), which energy delay product (EDP) is the most important parameter for optimization of VLSI circuits. Each proposed structure of multiplier or adder unit has its own advantages/disadvantages.

The total power dissipated in generic digital CMOS gate is calculated by Equation (1), Equation (2), Equation (3), and Equation (4).

$$P_{Total} = P_{Dynamic} + P_{Short\ Circuit} + P_{Static} \quad (1)$$

$$P_{Dynamic} = P.\ C_L.\ f.\ V_{DD}^2 \quad (2)$$

$$P_{Short\ Circuit} = I_{Peak}.\ t_{SC}.\ V_{DD}.\ f \quad (3)$$

$$P_{Static} = I_{Static}.\ V_{DD} \quad (4)$$

The above equations P, f, C_L, V_{DD}, I_{peak}, t_{SC} and I_{Static} are respectively, change state probability of gate, simulation frequency, capacitor of gate, supply voltage, and maximum current during changing the status of gate, short circuit time and static current. Static power is very important in low supply voltage.

Since input data for getting to output should pass of several adder units so output data have very high delay, moreover glitch effect exists either, that cause increasing its power. For removing these problems should reduce number of these units.

In the present paper, a new structure of multiplier is proposed to implement a 4*4 bit multiplier circuit. Our proposed structure is designed with minimum adder units' count, so it has the lowest power consumption, delay, PDP, EDP, area. This paper describes the design of a new structure for multipliers in digital applications, such as those used in DSP algorithms and cryptography. The proposed multiplier structure is simulated and the results are compared with other structures of multiplier such as Ripple Carry Array multiplier (RCA), Array multiplier, Braun multiplier and bypassing multiplier based on CSA and RCA. To simulating all of these structures are used 28T full adder cell. Based on the simulation results, our proposed structure of multiplier is the best structure of multiplier.

The remaining of the paper is organized as follows: The 28T full adder cell is described in Section (II). Illustration of multiplier architectures are shown in Section (III). Section (IV) is about the proposed multiplier based on a new (GCA multiplier). The simulation results of the proposed multiplier structure and its performance comparisons with counterparts' multipliers are shown in Section (V). Finally, conclusion is given in Section (VI).

II. CONVENTIONAL CMOS 28 TRANSISTOR (28T) FULL ADDER

The 28 transistor full adder is the pioneer CMOS traditional adder circuits. The schematic of this adder is shown in Fig. 1. This adder cell is built using equal number of NMOS and PMOS transistors. The main advantage this adder has completely output swing.

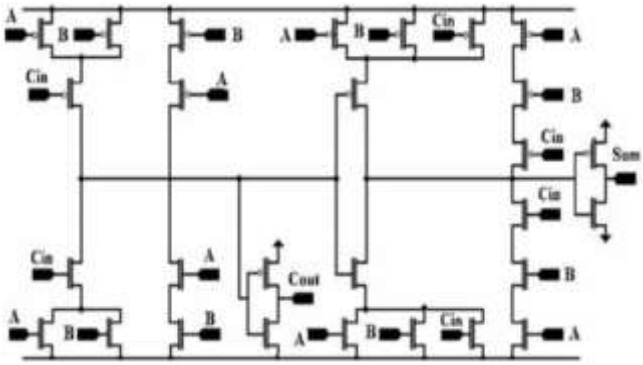

Figure 1. Conventional CMOS Adder with 28 transistors. Reprinted with permission from [12], J. M. Rabaey et al., Digital Integrated Circuits, Prentice Hall Publications (2003).

III. MULTIPLIER STRUCTURES

Multipliers are in fact complex adder arrays. This is a common operation to a large number of applications, and the complexity of this function has led to a large amount of research directed at speeding up its execution. Multiplier can be implemented using different algorithms. Some of common structures of multipliers are as shown in Fig. 2, Fig. 3, Fig. 4, Fig. 5, and Fig. 6.

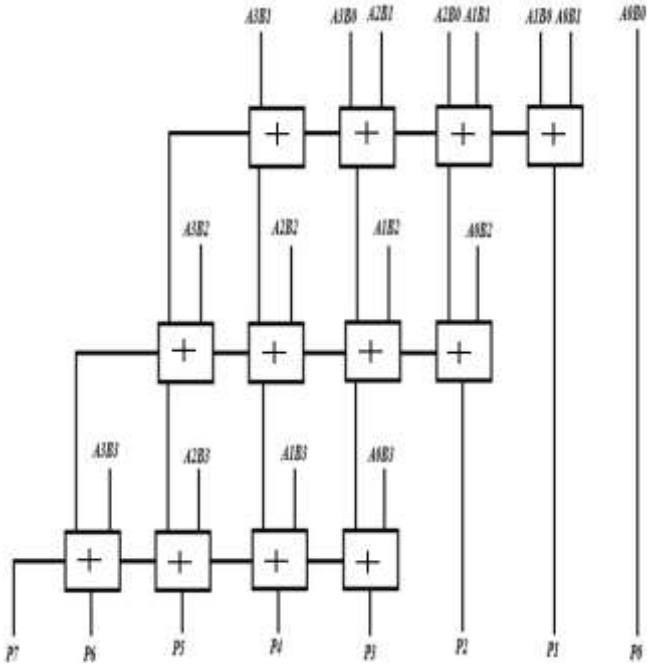

Figure 2. 4*4 Bit Array Multiplier

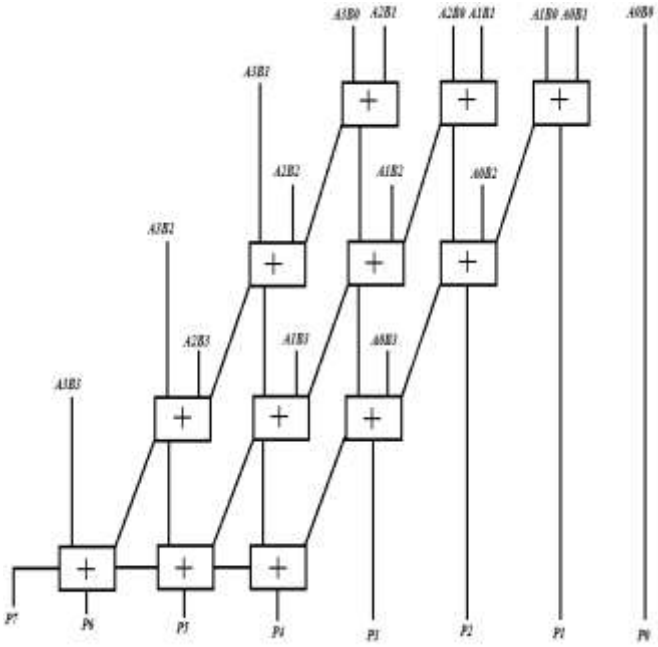

Figure 3. 4*4 Bit Basic Braun Multiplier

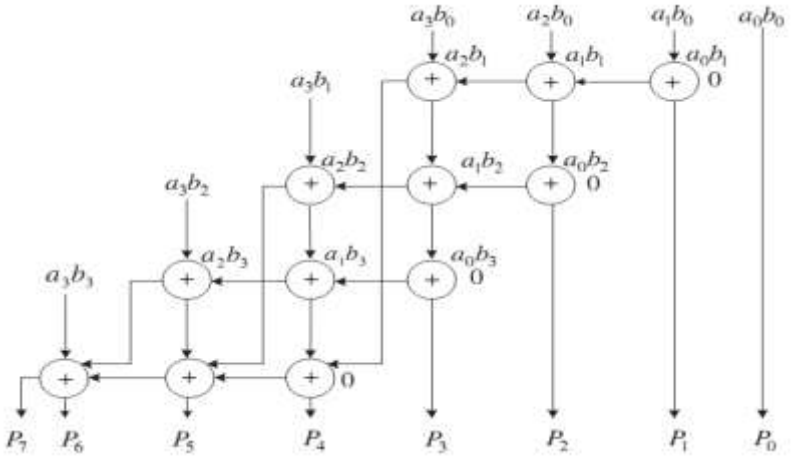

Figure 4. 4*4 Bit Ripple Carry Array Multiplier (RCA)

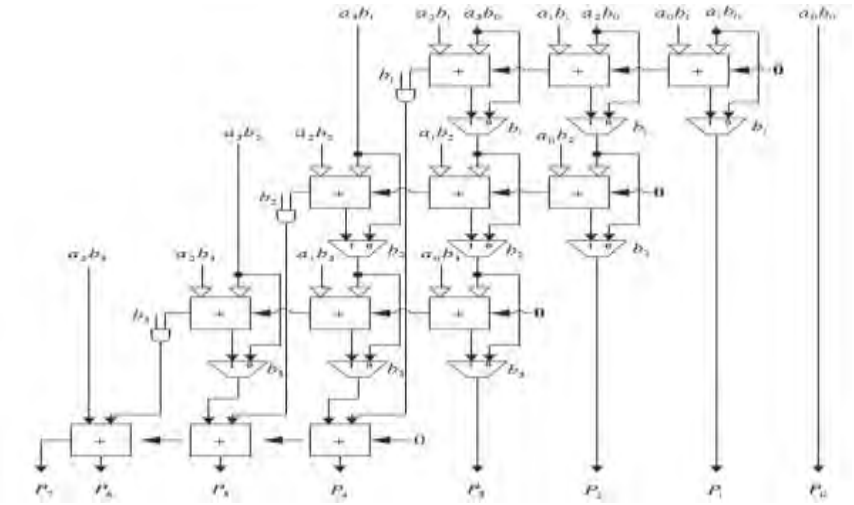

Figure 5. 4*4 Bit Row Bypassing Multiplier based on RCA

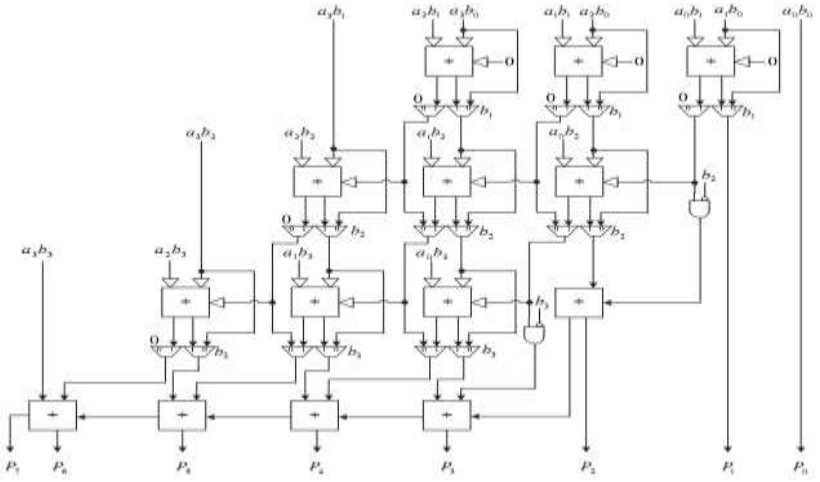

Figure 6. 4*4 Bit Bypassing Multiplier based on CSA

IV. PROPOSED MULTIPLIER BASED ON A NEW STRUCTURE (GCA MULTIPLIER)

In this section the novel structure of multiplier (GCA) is presented. In this structure are used minimum adder units, so it has the fewest transistor count than other structures. The Gyration Carry Array Multiplier (GCA) is as designed that it has very low propagation delay and power consumption, so we achieve to very low PDP and EDP. GCA multiplier is as shown in Fig. 7.

V. SIMULATIONS AND RESULTS

In this section, the proposed circuit is evaluated and compared to the other ones. All multipliers are simulated by using 28T full adder cell in 0.18µm CMOS technology files with 100MHz and at 27^0C and the supply voltage is 1.8 V. the simulation results of different multipliers and proposed multiplier (GCA multiplier) are tabulated in Table I.

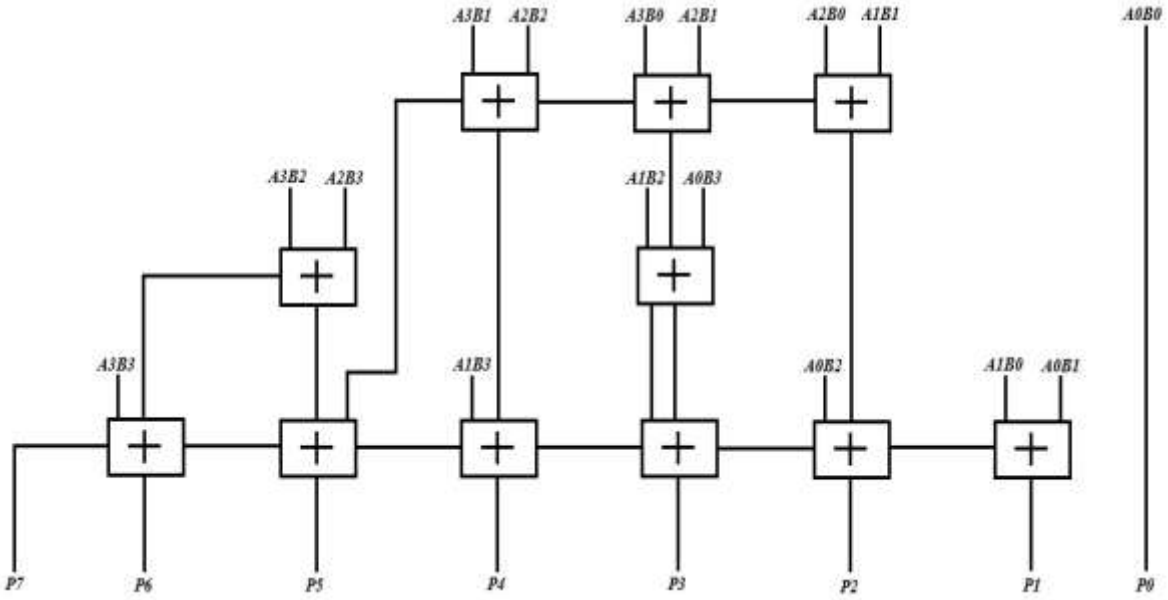

Figure 7. 4*4 Bit Gyration Carry Array Multiplier (GCA)

TABLE I. SIMULATION RESULT FOR MULTIPLIER IN 0.18 µM TECHNOLOGY WITH SUPPLY VOLTAGE AND FREQUENCY 1.8V, 100MHZ RESPECTIVELY

Design	Average power (µW)	Delay (PS)	PDP (FJ)	EDP ($*10^{-25}$)	Trans. Count
Array Multiplier	126.66	517.5	65.54655	339.2033	464
Braun Multiplier	125.76	526.5	66.21264	348.6095	464
RCA Multiplier	126.60	521.5	66.0219	344.304	464
Bypassing RCA Multiplier	164.84	509	83.90356	427.069	655
Bypassing CSA Multiplier	202.3	505.5	102.2626	516.937	810
Proposed Multiplier(GCA)	125.18	348	43.5626	151.5978	436

The results shows that the GCA multiplier consumes the least power compare to the others. Moreover GCA multiplier has the lowest propagation delay, power delay product, energy delay product and area than the other structures.

VI. CONCLUSIONS

In this paper a low power and high performance CMOS array multiplier is presented. The proposed multiplier reduces power consumption and propagation delay by remove extra adder units. This work primarily focused on the designing multiplier by using minimum adder units with minimum propagation delay. Intensively, HSPICE simulation shows that the new structure has the lowest power consumption, propagation delay, PDP, EDP. These results were obtained with simulating by HSPICE software at room temperature and supply voltage 1.8V.

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